In the Claims

Kindly submit the following claims with the present continuing application while repeating none of the claims from previous filed applications.

1. An interconnect structure S containing a plurality of nodes and a plurality of interconnects selectively coupling the nodes, the interconnect structure S comprising:

a node set T;

an interconnect set I that selectively connects nodes in the node set T;

a device set A mutually exclusive of the node set T with the devices in device set A being capable of sending data to one or more nodes in the node set T;

a device set Z mutually exclusive of the node set T with the devices in device set Z being capable of receiving data from one or more nodes in the node set T; and

a collection C of node subsets of the node set T, each node in the node set T being contained in exactly one member of the collection C such that:

for a device x in the device set Z, a sequence $cx = cx_0, cx_1, cx_2,..., cx_J$ exists with each member of the sequence cx being a node set in the collection C, the sequence cx being capable of passing data from devices in the device set A to the device x on a plurality of paths, among the plurality of paths being a path set P(x) characterized in that a path R is included in the path set P(x) only if each node on the path R is in a member of the sequence cx, a node of the path R that receives a message directly from a device in device set A being a member of node set cx_U and a node of the path R that sends data directly to the device x being a member of node set cx_V with U being larger than V;

for a member Y of the collection C, a corresponding set of devices Z(Y) exists in the device plurality Z such that a device y is included in the set of devices Z(Y) only if the member Y is also a member of the sequence cy;

for members cx_H and cx_K of the sequence cx with $H > K$, a device set $Z(cx_K)$ is a subset of a device set $Z(cx_H)$;

the sequence cx includes two members cx_L and cx_m with L>M and with the device set $Z(cx_M)$ being a subset of a device set $Z(cx_L)$ and a device exists in the device set $Z(cx_L)$ that is not included in the device set $Z(cx_M)$; and

the node set T includes three distinct nodes p, q, and r, the node p being in a member cx_D of the sequence cx, the nodes q and r being in a member cx_E of the sequence cx with D > E, in one path of the plurality of paths P(x) a message moves directly from the node p to the node r and in another path of the plurality of paths P(x) a message moves directly from the node q to the node r.

2. An interconnect structure according to Claim 1 wherein:

the plurality of paths of the sequence cx include a path such that if a message hops from a node in a member cx_n to a node in a member cx_m, then n > m.

3. An interconnect structure according to Claim 1 further comprising:

an arrangement of the nodes in the interconnect structure into a hierarchy of levels of node sets $LV = LV_0, LV_1, \ldots LV_J$, each member of the hierarchy LV being a node set that is subset of the node set T and each node in the node set T is contained in exactly one member of the node sets LV; and

for the device x of the device set Z, a node set cx_N is a subset of the level N node set L_N, with N not exceeding J.

4. An interconnect structure according to Claim 3 wherein:

the collection C includes 2^{J-N} members on a level N;

the collection C includes three members D, E and F such that member node set D is on the level LV_N and member node sets E and F are on the level LV_{N-1};

the interconnect set I includes interconnects positioned to allow data to pass directly from the member node set D to the member node set E and to pass directly from the node set D to the node set F; and

the device set Z includes device sets Z(D), Z(E), and Z(F) that correspond to the three members D, E, and F, the device sets Z(E) and Z(F) being mutually exclusive device sets, and device set Z(D) is the union of the device sets Z(E) and Z(F).

5. An interconnect structure according to Claim 1 further comprising:

a logic L_p associated with the node p wherein for a message Mp that arrives at the node p, the logic Lp uses information concerning the sending of messages from node q for the logic Lp to determine where the node pis to send the message Mp.

6. An interconnect structure according to Claim 1 wherein:

the node q has priority over the node p to send data to the node r so that a message Mq located at the node q is not blocked from being sent to the node r by a message Mp at the node p; and

the node q is capable of sending a control signal to the node p wherein the purpose of the control signal is to enforce the priority of the node q over the node p to send data to the node r.

7. An interconnect structure according to Claim 1 wherein:

the node set T includes a node s distinct from the nodes p, q, and r, the node s being in the member cx_D, so that in one path of the plurality of paths P(x), a message moves from the node P directly to the node s.

8. An interconnect structure comprising:

a plurality of nodes including a node N_E and a node set P, the node set P including a plurality of nodes that are capable of sending data to the node N_E; and

a plurality of interconnect paths interconnecting the plurality of nodes, the interconnect paths including data interconnect paths that couple nodes in pairs, a node pair including a sending node and a receiving node, the sending node being capable of sending data to the receiving node;

the nodes in the node set P having a priority relationship for sending data to the node N_E, the nodes in the node set P including distinct nodes N_F and N_A, the node N_F having a highest priority among the nodes in the node set P for sending data to the node N_E so that a message M_F arriving at the node N_F is not blocked from traveling to the node N_E by a message M_A arriving at the node N_A; and

for a message M arriving at the node N_A and the message M is blocked from being sent to the node N_E, then the blocking of the message M from being sent to the node N_E causes sending of the message M from the node N_A to a node distinct from the node N_E.

9. An interconnect structure according to Claim 8 wherein:

the priority relationship among the nodes in the node set P capable of sending data to the node N_E depends on the position of the individual nodes in the node set P within the interconnect structure.

10. An interconnect structure according to Claim 8 further comprising:

the plurality of nodes including the distinct nodes N_A, N_E, and N_F; a plurality of logic elements associated with the plurality of nodes;

a plurality of data interconnect paths coupling the plurality of nodes, a data interconnect path coupling the plurality of nodes in pairs including a receiving node and a sending node capable of sending data to the receiving node;

a plurality of control signal interconnect paths coupling the plurality of nodes to send a control signal from a source associated with the sending node to a logic element associated with the receiving node;

the plurality of nodes including:

a logic L_A associated with the node N_A that makes routing decisions for the node N_A;

a data interconnect path from the node N_F operative as the sending node to the node N_E operative as the receiving node;

a data interconnect path from the node N_A operative as the sending node to the node N_E operative as the receiving node; and

a control signal interconnect path from a source associated with the node N_F operative as a sending node to the logic L_A, the control signal enforcing a priority for sending data from the node N_F to the node N_E over sending data from the node N_A to the node N_E.

11. An interconnect structure according to Claim 8 further comprising:

the plurality of nodes including the node N_F, the node N_A, and a node set R, the nodes N_F and NA being distinct nodes that are excluded from the node set R, the node N_A being capable of sending data to each node in the node set R;

the plurality of data interconnect paths coupling the plurality of nodes, a data interconnect path coupling a pair of the plurality of nodes as a sending node capable of sending data to a receiving node; and

the plurality of control interconnect paths coupling the plurality of nodes, a control interconnect path used to carry control signals from a source associated with a control signal sending node to a logic associated with a control signal using node, the plurality of control interconnect paths including a control interconnect path from a source associated with the node N_F to the logic L_A associated with the node N_A, the logic L_A using a control signal from a source associated with the node N_F to determine to which node of the node set R the node N_A sends data.

12. An interconnect structure according to Claim 8 further comprising:

the plurality of nodes include the nodes N_A, N_D; N_E, and N_F;

the interconnect paths include control interconnect paths and data interconnect paths, the control interconnect paths capable of sending a control signal from a source associated with a control-signal-sending node to a logic associated with a control- signal-using node, the data interconnect paths capable of sending data from a data sending node to a data receiving node;

the plurality of interconnect paths further include data interconnect paths for sending data from the node N_A to the node N_E and to the node N_D, and a control interconnect path for sending a control signal from a source associated with the node N_F to the logic element L_A associated with node N_A, and

for a message M arriving at the node N_F, a source associated with the node N_F sends a control signal S to the logic element L_A, the logic element L_A using the control signal S to determine between sending the message M to the node N_E or to the node N_D.

13. An interconnect structure according to Claim 8 further comprising:

the plurality of nodes including input data ports, output data ports, and a plurality of logical elements that control the flow of data through the nodes, the plurality of nodes including distinct nodes N_F, N_A, N_E, and N_D;

the plurality of data-carrying interconnect paths coupling the plurality of nodes to form paths from the output data ports of data sending nodes to the input data ports of data receiving nodes;

the plurality of control signal interconnect paths for sending control signals to a logical element associated with a node having a data flow that depends on the control signals; and

a logical element L_A associated with the node N_A, the logical element L_A that uses a control signal from a source associated with the node N_F to determine where to route a message M passing through the node N_A, a control signal S received from a source associated with the node N_F that causes sending of the message M from the node N_A to the node N_E, and a control signal S' received from the node N_F that causes sending of the message M from the node N_A to the node N_D.

14. An interconnect structure according to Claim 8 wherein:

when a message M arrives at the node N_A and is targeted for the node N_E and not blocked by a message M' arriving at a node in the node set P having a higher priority than the node N_A for sending messages to the node N_E, the node N_A sends the message M to the node N_E.

15. An interconnect structure S containing a plurality of nodes and a plurality of interconnects selectively coupling the nodes, the interconnect structure comprising:

a node set T;

an interconnect set I that selectively connects nodes in the node set T;

a device set A mutually exclusive with the node set T with each device in device set A capable of sending data to a node in node set T;

a device set Z mutually exclusive with the node set T with each device in device set Z capable of receiving data from a node in node set T;

a set of data-carrying paths P, each path of path set P being capable of carrying data from a device in the device set A to a device in the device set Z, each node on the path of path set P is included in the node set T, and each interconnect in the path is included in the interconnect set I;

a node set U characterized as the set of nodes within the node set T that are on a path included in the path set P;

for a node N in the node set T such that the node N is on a path in the path set P, a corresponding set of devices Z(N) exists in the device set Z such that a device w is, included in the device set Z(N) only if a path exists in the path set P from a member of the device set A to the device w such that the path contains the node N; and

the node set U includes three distinct nodes N_A, N_D, and N_E such that node N_A is capable of sending data to node N_D and node N_E, and device set $Z(N_A)$ is the same as device set $Z(N_D)$, and device set $Z(N_E)$ is a proper subset of device set $Z(N_A)$.

16. An interconnect structure according to Claim 15 wherein:

a time T_A is associated with the node N_A such that messages arriving at the node N_A are sent to another node within the time T_A of the messages' arrival at the node N_A.

17. An interconnect structure according to Claim 15 further comprising:

a logic element L_A associated with the node N_A that determines routing from the node N_A;

a node N_X distinct from the node N_A; and

a logical element L_X associated with the node N_X that determines routing for the node N_X, the logical element L_X being distinct from the logical element L_A.

18. An interconnect structure according to Claim 15 further comprising:

the plurality of nodes including a node N_F, the nodes N_A, N_E, and N_F being mutually distinct;

a plurality of logic elements associated with the plurality of nodes;

a plurality of data interconnect paths coupling the plurality of nodes, a data interconnect path coupling the plurality of nodes in pairs including a receiving node and a sending node capable of sending data to the receiving node;

a plurality of control signal interconnect paths coupling the plurality of nodes to send a control signal from a source associated with the sending node to a logic element associated with the receiving node;

the plurality of nodes including:

a logic L_A associated with the node N_A that makes routing decisions for the node N_A;

a data interconnect path from the node N_F operative as the sending node to the node N_E operative as the receiving node;

a data interconnect path from the node N_A operative as the sending node to the node N_E operative as the receiving node; and

a control signal interconnect path from a source associated with the node N_F operative as a sending node to the logic L_A, the control signal enforcing a priority for sending data from the node N_F to the node N_E over sending data from the node N_A to the node N_E.

19. An interconnect structure according to Claim 15 further comprising:

the plurality of nodes including a node N_F and a node set R, the nodes N_F and N_A being distinct nodes that are excluded from the node set R, the node N_A being capable of sending data to each node in the node set R;

the plurality of data interconnect paths coupling the plurality of nodes, a data interconnect path coupling a pair of the plurality of nodes as a sending node capable of sending data to a receiving node; and

the plurality of control interconnect paths coupling the plurality of nodes, a control interconnect path used to carry control signals from a source associated with a control signal sending node to a logic associated with a control signal using node, the plurality of control interconnect paths including a control interconnect path from a source

associated with the node N_F to the logic L_A associated with the node N_A, the logic L_A using a control signal from a source associated with the node N_F to determine to which node of the node set R the node N_A sends data.

20. An interconnect structure according to Claim 15 further comprising:

the plurality of nodes include a node N_F;

the interconnect paths include control interconnect paths and data interconnect paths, the control interconnect paths capable of sending a control signal from a source associated with a control-signal-sending node to a logic associated with a control- signal-using node, the data interconnect paths capable of sending data from a data sending node to a data receiving node;

the plurality of interconnect paths further include data interconnect paths for sending data from the node N_A to the node N_E and to the node N_D, and a control interconnect path for sending a control signal from a source associated with the node N_F to the logic element L_A associated with node N_A, and

for a message M arriving at the node N_F, a source associated with the node N_F sends a control signal S to the logic element L_A, the logic element L_A using the control signal S to determine between sending the message M to the node N_E or to the node N_D.

21. An interconnect structure according to Claim 20 wherein:

the control interconnect path from the node N_F to the node N_A is a direct link from a logic L_F associated with the node N_F to the logic L_A.

22. An interconnect structure according to Claim 20 wherein:

the control signal sent to the node N_A is tapped from an output data port of the node N_F.

23. An interconnect structure according to Claim 15 further comprising:

the plurality of nodes including input data ports, output data ports, and a plurality of logical elements that control the flow of data through the nodes, the plurality of nodes including a node N_F, the nodes N_F, N_A, N_E, and N_D being mutually distinct;

the plurality of data-carrying interconnect paths coupling the plurality of nodes to form paths from the output data ports of data sending nodes to the input data ports of data receiving nodes;

the plurality of control signal interconnect paths for sending control signals to a logical element associated with a node having a data flow that depends on the control signals; and

a logical element L_A associated with the node N_A, the logical element L_A that uses a control signal from a source associated with the node N_F to determine where to route a message M passing through the node N_A, a control signal S received from a source associated with the node N_F that causes sending of the message M from the node N_A to the node N_E, and a control signal S' received from the node N_F that causes sending of the message M from the node N_A to the node N_D.

24. An interconnect structure according to Claim 15 further comprising:

an interconnect link IL in interconnect set I, the interconnect link IL being an interconnect link on a path in the path set P such that a corresponding set of devices Z(IL) exists in the device set Z such that a device w is included in the device set Z(IL) only if a path containing the interconnect link IL in the path set P exists from a device in the device set A to the device w; and

the node set. U includes distinct nodes N_A, N_D, and N_E such that node N_A is capable of sending data to the node N_D on a link L_{AD}, the node N_A is capable of sending data to the node N_E on a link L_{AE}, and the device set $Z(L_{AE})$ is a proper subset of the device subset $Z(L_{AD})$.

25. An interconnect structure comprising:

a plurality of interconnected nodes including distinct nodes N_F, N_A and N_E;

means for sending a plurality of messages including a message M_F and a message M_A through the interconnected nodes;

means for routing the message M_F to enter the node N_F;

means for routing the message M_A to enter the node N_A; and

means for using information concerning the routing of the message M_F through the node N_F to the node N_E to route the message M_A through the node N_A.

26. An interconnect structure according to Claim 25 further comprising:

a plurality of logic elements associated with the plurality of nodes;

a plurality of message interconnect paths coupling the plurality of nodes, a message interconnect path coupling a pair of the plurality of nodes as a sending node and a receiving node, the sending node being capable of sending data to a receiving node;

a plurality of control signal interconnect paths coupling the plurality of nodes to send a control signal from a source associated with a sending node to a logic element associated with a control signal using node;

the plurality of nodes including:

distinct nodes N_F, N_A and N_E;

a logic L_A associated with the node N_A that makes routing decisions for the node N_A;

a message interconnect path from the node N_F operative as a sending node for sending a message to the node N_E operative as a receiving node;

a message interconnect path from the node N_A operative as a sending node for sending a message to the node N_E operative as a receiving node; and

a control signal interconnect path connected from a source associated with the node N_F to the logic L_A, the node N_F operative as a sending node for sending a control signal to the logic L_A, the control signal enforcing a priority for sending data from the node N_F to the node N_E over sending data from the node N_A to the node N_E.

27. An interconnect structure according to Claim 25 further comprising:

the plurality of nodes including the node N_F, the node N_A, and a node set P, the nodes N_F and N_A being distinct nodes that are excluded from the node set P, the node N_A being capable of sending data to each node in the node set P;

a plurality of data interconnect paths coupling the plurality of nodes, a data interconnect path coupling a pair of the plurality of nodes as a sending node capable of sending data to a receiving node; and

a plurality of control interconnect paths coupling the plurality of nodes, a control interconnect path used to carry control signals from a source associated with a control signal sending node to a logic associated with a control signal using node, the plurality of control interconnect paths including a control interconnect path from a source associated with the node N_F to a logic L_A associated with the node N_A; the logic L_A using a control signal from a source associated with the node N_F to determine to which node of the node set P the node N_A sends data.

28. An interconnect structure according to Claim 25 further comprising:

the plurality of nodes including the node N_F, the node N_A, the node N_E, and a node N_D that are mutually distinct;

a plurality of interconnect paths, the interconnect paths including control interconnect paths" and data interconnect paths, the control interconnect paths capable of sending a control signal from a source associated with a control-signal-sending node to a logic associated with a control-signal-using node, the data interconnect paths capable of sending data from data sending nodes to data receiving nodes;

the plurality of interconnect paths further including data interconnect paths for sending data from the node N_A to the node N_E and to the node N_D, and a control interconnect path for sending a control signal from a source associated with the node N_F to a logic element L_A associated with node N_A, wherein

for a message M arriving at the node N_A, a source associated with the node N_F sends a control signal S to the logic element L_A, the logic element L_A using the control signal S to determine between sending the message M to the node N_E or to the node N_D.

29. An interconnect structure according to Claim 25 further comprising:

the plurality of nodes including input data ports, output data ports, and a plurality of logical elements that control the flow of data through the nodes, the plurality of nodes including distinct nodes N_F, N_A, N_E, and N_D;

a plurality of data-carrying interconnect paths coupling the plurality of nodes to form paths from the output data ports of data sending nodes to the input data ports of data receiving nodes;

a plurality of control signal interconnect paths for sending control signals to logical elements associated with nodes having a data flow that depends on the control signals,

the node N_A associated with a logical element L_A that uses a control signal from a source associated with the node N_F to determine where to route a message M passing through the node N_A, a control signal S received from a source associated with the node N_F causing sending of the message M from the node N_A to the node N_E, and a control signal S' received from the node N_F causing sending of the message M from the node N_A to the node N_D.

30. An interconnect structure according to Claim 25 further comprising:

the plurality of nodes including the node N_E and a node set P, the node set P including a plurality of nodes that are capable of sending data to the node N_E;

a plurality of interconnect paths coupling the plurality of nodes, the interconnect paths including data interconnect paths, a data interconnect path coupling a pair of the plurality of nodes as a sending node capable of sending data to a receiving node;

the nodes in the node set P having a priority relationship for sending data to the node N_E in which a node N_F exists that. has a highest priority for sending data to the node N_E so that data arriving at the node N_F is not blocked from traveling to the node N_E by a message traveling to the node N_E from a node in the node set P distinct from the node N_F; and

the node N_A being a node in the node set P such that the node N_A is distinct from the nodes N_F and N_E and such that the node N_A is capable of sending data to the node N_E and the node N_A is capable of sending data to a node N_D distinct from the node N_E.

31. An interconnect structure according to Claim 30 wherein:

the priority relationship among the nodes in the node set P capable of sending data to the node NE depends on the position of the individual nodes in the node set P within the interconnect structure.

32. An interconnect structure according to Claim 25 further comprising:

the plurality of nodes including the node N_E and a node set P, the node set P including a plurality of nodes that are capable of sending data to the node N_E;

a plurality of interconnect paths coupling the plurality of nodes, the interconnect paths including data interconnect paths, a data interconnect path coupling a pair of the plurality of nodes as a sending node capable of sending data to a receiving node;

the nodes in the node set P having a priority relationship for sending data to the node N_E in which a node N_F exists that has a highest priority for sending data to the node N_E so that data arriving at the node N_F is not blocked from traveling to the node N_E by a message traveling to the node N_E from a node in the node set P distinct from the node N_F; and

the node N_A being a node in the node set P such that the node N_A is distinct from the node N_F so that if a message M arrives at the node N_A and the message M is blocked from being sent to the node N_E, then the blocking of message M from being sent to the node N_E causes sending of the message M from the node N_A to a node distinct from the node N_E.

33. An interconnect structure according to Claim 25 further comprising:

the plurality of nodes including the node N_E and a node set P, the node set P including a plurality of nodes that are capable of sending data to the node N_E; and

a plurality of interconnect paths coupling the plurality of nodes, the interconnect paths including data interconnect paths, a data interconnect path coupling a pair of the plurality of nodes as a sending node capable of sending data to a receiving node; and

the nodes in the node set P having a priority relationship for sending data to the node N_E in which a node N_F exists that has a highest priority for sending data to the node N_E so that data arriving at the node N_F is not blocked from traveling to the node N_E by a message

traveling to the node N_E from a node in the node set P distinct from the node N_F, the node N_A being a node in the node set P such that the node N_A is distinct from the node N_F and is capable of sending messages to the node N_E, wherein:

when a message M arrives at the node N_A, and is targeted for the node N_E and not blocked by a message M' arriving at a node in the node set P having a higher priority than the node N_A for sending messages to the node N_E, the node N_A sends the message M to the node N_E.

34. An interconnect structure comprising:

a plurality of nodes that function as data sending nodes, data receiving nodes, or both data sending and data receiving nodes, the plurality of nodes including a node N_F, a node N_A, a node N_E, and a node N_D that are mutually distinct;

a plurality of interconnect paths that are capable of carrying data from a node currently functioning as a data sending node to a node currently functioning as a data receiving node, the interconnect paths including a data interconnect path for carrying data from the node N_A to the node N_E and a data interconnect path for carrying data from the node N_A to the node N_D, the interconnect paths including at least two data interconnect paths for usage in carrying data from the node N_F; and

a control logic wherein, for a message M_A routed through the node N_A and a message M_F routed through the node N_F to a receiving node that is not the node N_A, information concerning routing of the message M_F through the node N_F is used to determine control information C;

if information C has a value C_1, then the message M_A is routed from the node N_A through the node N_D;

if information C has a value C_2, then the message M_A is routed from the node N_A through the node N_E.

35. An interconnect structure according to Claim 34 further comprising:

the plurality of nodes including the node N_F, the node N_A, and a node set P, the nodes N_F and N_A being distinct nodes that are outside of the node set P, the node N_A being capable of sending data to each node in the node set P;

the plurality of data interconnect paths coupling the plurality of nodes, a data interconnect path coupling a pair of the plurality of nodes as a sending node capable of sending data to a receiving node; and

the plurality of control interconnect paths coupling the plurality of nodes, a control interconnect path used to carry control signals from a source associated with a control signal sending node to a logic associated with a control signal using node, the plurality of control interconnect paths including a control interconnect path from a source associated with the node N_F to a logic L_A associated with the node N_A; the logic L_A using a control signal from a source associated with the node N_F to determine to which node of the node set P the node N_A sends data.

36. An interconnect structure S comprising:

a plurality of nodes including nodes N_A, N_D, and N_E;

a plurality of interconnect lines selectively coupling the nodes in the structure S;

a plurality of devices in a device set I that is mutually exclusive of the plurality of nodes, the devices in the device set I being capable of sending data to one or more of the plurality of nodes; and

a plurality of devices in a device set Z that is mutually exclusive of the plurality of nodes, the devices in the device set Z being capable of receiving data from one or more of the plurality of nodes, the device set Z comprising a plurality of device subsets further comprising:

a device subset T_A consisting of devices t_A such that a message can be sent from a device in device set I through the node N_A to the device t_A;

a device subset T_D consisting of devices t_D such that a message can be sent from a device in device set I through the node N_D to the device t_D; and

a device subset T_E consisting of devices t_E such that a message can be sent from a device in device set I through the node N_E to the device t_E;

wherein:

the node N_A is capable of sending data to the node N_D;

the node N_A is capable of sending data to the node N_E;

the devices in the device subset T_A are included in the device subset T_D; and

a device t_A exists that is included in the device subset T_A and excluded from the device subset T_E.

37. An interconnect structure S according to Claim 36 further comprising:

a logic L capable of controlling passage of messages sent through the interconnect structure S, wherein:

a plurality of messages P can be sent to a plurality of nodes from a plurality of devices in the device set I;

the plurality of messages P includes a message M_A having a target device in the device subset T_A; and

the logic L is capable of routing the message M_A through the node N_A to a device in the device subset T_A.

38. An interconnect structure S according to Claim 36 wherein:

the message M_A has a header; and

the logic L is capable of routing the message M_A through the interconnect structure S using information in the header of the message M_A.

39. An interconnect structure S according to Claim 36 wherein:

the logic L is distributed among one or more nodes of the plurality of nodes;

the plurality of nodes includes a node N; and

logic of the logic L associated with the node N uses control signals to route messages through the node N.

40. An interconnect structure S containing a plurality of nodes and a plurality of interconnects selectively coupling the nodes, the interconnect structure S comprising:

a node set T including three distinct nodes N_A, N_D, and N_E;

a device set I mutually exclusive of the node set T and containing devices capable of sending data to at least one node in the node set T;

a device set Z mutually exclusive of the node set T and containing devices capable of receiving data from at least one node in the node set T;

a plurality of paths P capable of carrying data through the interconnect structure S to devices in the device set Z;

a device subset T_A exists such that a message can be sent on a path in the path set P from a device in the device set I through the node N_A to the device in the device subset T_A;

a device subset T_D exists such that a message can be sent on a path in the path set P from a device in the device set I through the node N_D to the device in the device subset T_D;

a device subset T_E exists such that a message can be sent on a path in the path set P from a device in the device set I through the node N_E to the device in the device subset T_E;

wherein:

the node N_A is capable of sending data to the node N_D along a path in the path set P;

the node N_A is capable of sending data to the node N_E along a path in the path set P;

the devices in the device subset T_A are included in the device subset T_D; and

a device exists that is included in the device subset T_A that is not included in the device subset T_E.

41. An interconnect structure S according to Claim 40 further comprising:

a logic L_A associated with the node N_A controls data flow from the node N_A.

42. An interconnect structure S containing a plurality of nodes and a plurality of interconnects selectively coupling the nodes, the interconnect structure S comprising:

a node set T including three distinct nodes N_A, N_C, and N_E;

a device set I mutually exclusive of the node set T and containing devices capable of sending data to at least one node in the node set T;

a device set Z mutually exclusive of the node set T and containing devices capable of receiving data from at least one node in the node set T;

a plurality of paths P capable of carrying data through the interconnect structure S to devices in the device set Z;

a device subset T_A exists such that a message can be sent on a path in the path set P from a device in the device set I through the node N_A to the device in the device subset T_A;

a device subset T_C exists such that a message can be sent on a path in the path set P from a device in the device set I through the node N_C to the device in the device subset T_C;

a device subset T_E exists such that a message can be sent on a path in the path set P from a device in the device set I through the node N_E to the device in the device subset T_E;

wherein:

the node N_C is capable of sending data to the node N_E along a path in the path set P;

the node N_A is capable of sending data to the node N_E along a path in the path set P;

the devices in the device subset T_C are included in the device subset T_E; and

a device exists that is included in the device subset T_A that is not included in the device subset T_E.

43. An interconnect structure S according to Claim 42 further comprising:

a logic L_A associated with the node N_A controls data flow from the node N_A.

44. An interconnect structure S according to Claim 43 wherein:

a message M arriving at the node N_A has a header and the logic L_A uses information in the header to decide where to send the message M.

45. An interconnect structure S according to Claim 43 wherein:

the logic L_A uses information from the node N_C to decide where to send the message M.